Electronic Version
Stylesheet Version v1.1.1

[FLASH MEMORY STRUCTURE AND OPERATING METHOD THEREOF]

Abstract

A flash memory structure is provided. The flash memory structure includes a P-type substrate, a deep N-well set up within the P-type substrate, a P-well set up within the deep N-well, a pair of gate structures set up over the substrate, a select gate set up between the pair of gate structure and N-type source/drain regions in the P-well on each side of the gate structure. Since each pair of neighboring gate structure uses a common gate, the level of integration of device can be increased.